REMARKS

Upon entry of the instant Amendment, claims 1-22, 24, 25 and 31-47 will be pending in the application. By this amendment, claim 38 will have been amended. No new matter is added. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

35 U.S.C. § 103 Rejections

Over Gardner with Murthy

Claims 1, 3-5, 9-18 and 31-37 (an presumably also claims 24 and 25) were rejected under 35 U.S.C. § 103(a) for being allegedly unpatentable over U.S. Patent No. 6,111,292 to GARDNER et al. in view of U.S. Patent No. 6,621,131 to MURTHY et al. This rejection is respectfully traversed.

The Examiner acknowledges that GARDNER fails to disclose, among other things, filling a first portion of the recesses with a stress imposing material and filling a second portion of the recesses with a semiconductor material (claim 1). The Examiner also acknowledges that GARDNER fails to disclose, among other things, filling a first portion of the first recess and a first portion of the second recess with a stress imposing material configured to enhance performance of the field effect transistor gate and filling a second portion of the first recess and a second portion of the second recess for the field effect transistor gate with a semiconductor material (claim 31). However, the Examiner explains that these features are taught by MURTHY and that it would have been obvious to combine the teachings of these documents to achieve the claimed invention.

Applicants respectfully submit that a *prima facie* case of obviousness has not been established as the applied references fail to teach each and every element of the claims.

Applicants acknowledge that GARDNER discloses a device which forms LDD areas 48 within spacer openings 46 and in the substrate 30 (see col. 7, lines 41-56 and Figs. 7-17). However, the Examiner is not correct that GARDNER discloses recesses arranged below spacer voids 46. Reference numbers 48 in Fig. 9 of GARDNER are disclosed as being formed LDD areas (see col. 7, lines 41-56) and not recesses. Furthermore, as correctly acknowledged by the Examiner, GARDNER also fails to disclose or suggest filling a first portion of the recesses with a stress imposing material and filling a second portion of the recesses with a semiconductor material (claim 1) and/or filling a first portion of the first recess and a first portion of the second recess with a stress imposing material configured to enhance performance of the field effect transistor gate and filling a second portion of the first recess and a second portion of the second recess for the field effect transistor gate with a semiconductor material (claim 31).

MURTHY does not cure the deficiencies of GARDNER, however. While it is apparent that MURTHY discloses a device having recesses 36A and 36B with surfaces 38 and that are filled with materials 40A and 40B (see Figs. 5-6 and col. 3, lines 27-59), it is clear that the recesses 36A and 36B are not arranged below spacer voids. To the contrary, MURTHY discloses spacers 26A and 26B which have regions 22A and 22B underneath. There are no voids underneath spacers 26A and 26B. Accordingly, the Examiner simply cannot properly argue that MUTHRY discloses or suggests filling a first

portion of the recesses with a stress imposing material and filling a second portion of the recesses with a semiconductor material (claim 1) and/or filling a first portion of the first recess and a first portion of the second recess with a stress imposing material configured to enhance performance of the field effect transistor gate and filling a second portion of the first recess and a second portion of the second recess for the field effect transistor gate with a semiconductor material (claim 31).

Accordingly, Applicants submit that no proper combination of GARDNER and MURTHY discloses or suggests the combination of features recited in at least claims 1 and 31.

Moreover, in addition to failing to disclose the combination of features recited in the above-noted claims 1 and 31, Applicants submit no proper combination of these documents discloses or suggests the combination of features recited in dependent claims 2, 3-5, 9-18, 24, 25 and 32-37, which also respectfully contain all of the features of claims 1 and 31.

Accordingly, Applicants respectfully submit that the above-noted rejection under 35 U.S.C. § 103(a) should be withdrawn.

Over Gardner with Murthy and Yu

Claims 2 and 6-8 were rejected under 35 U.S.C. § 103(a) for being allegedly unpatentable over GARDNER in view of MURTHY and further in view of U.S. Patent No. 6,297,117 to YU. This rejection is respectfully traversed.

The Examiner acknowledges that GARDNER and MURTHY fails to disclose, among other things, the features recited in the above-noted dependent claims.

However, the Examiner explains that these features are taught by YU and that it would have been obvious to combine the teachings of these documents.

Applicants respectfully submit that a *prima facie* case of obviousness has not been established as the applied references fail to teach each and every element of the claims.

As explained above, while Applicants acknowledge that GARDNER discloses a device which forms LDD areas 48 within spacer openings 46 and in the substrate 30 (see col. 7, lines 41-56 and Figs. 7-17), GARDNER does not disclose recesses arranged below spacer voids 46. Again, reference numbers 48 in Fig. 9 of GARDNER are disclosed as being formed LDD areas (see col. 7, lines 41-56) and not recesses. Moreover, as correctly acknowledged by the Examiner, GARDNER fails to disclose or suggest filling a first portion of the recesses with a stress imposing material and filling a second portion of the recesses with a semiconductor material (claim 1).

Again, MURTHY does not cure the deficiencies of GARDNER. While it is apparent that MURTHY discloses a device having recesses 36A and 36B with surfaces 38 and that are filled with materials 40A and 40B (see Figs. 5-6 and col. 3, lines 27-59), it is clear that the recesses 36A and 36B are not arranged below spacer voids. To the contrary, MURTHY discloses spacers 26A and 26B which have regions 22A and 22B underneath. There are no voids underneath spacers 26A and 26B. Accordingly, the Examiner simply cannot properly argue that MUTHRY discloses or suggests filling a first portion of the recesses with a stress imposing material and filling a second portion of the recesses with a semiconductor material (claim 1).

YU does not cure the deficiencies of GARDNER and MURTHY. While it is apparent that YU discloses a device having regions 210/214 and 242/244 below spacer voids 232 and 234 (see Figs. 6-8), it is clear from Figs. 6-11 that the layers 228 prevent the spacers from penetrating into the substrate and that the disclosed device uses no recesses below the spacer voids 232 and 234. There are simply no voids underneath spacers 224 and 226. Accordingly, the Examiner simply cannot properly argue that YU discloses or suggests filling a first portion of the recesses with a stress imposing material and filling a second portion of the recesses with a semiconductor material (claim 1).

Accordingly, Applicants submit that no proper combination of GARDNER, MURTHY and YU discloses or suggests the combination of features recited in at least claim 1.

Moreover, in addition to failing to disclose the combination of features recited in the above-noted claim 1, Applicants submit no proper combination of these documents discloses or suggests the combination of features recited in dependent claims 2 and 6-8, which also respectfully contain all of the features of claim 1.

Accordingly, Applicants respectfully submit that the above-noted rejection under 35 U.S.C. § 103(a) should be withdrawn.

Over Yu with Gardner and Murthy

Claims 19-22 were rejected under 35 U.S.C. § 103(a) for being allegedly unpatentable over YU in view of GARDNER and MURTHY. This rejection is respectfully traversed.

The Examiner acknowledges that YU and GARDNER fails to disclose, among other things, filling a first filling a first portion of the recesses with a stress imposing material and filling a second portion of the recesses with a semiconductor material. However, the Examiner explains that these features are taught by MURTHY and that it would have been obvious to combine the teachings of these documents.

Applicants respectfully submit that a *prima facie* case of obviousness has not been established as the applied references fail to teach each and every element of the claims.

As explained above, while it is apparent that YU discloses a device having regions 210/214 and 242/244 below spacer voids 232 and 234 (see Figs. 6-8), it is clear from Figs. 6-11 that the layers 228 prevent the spacers from penetrating into the substrate and that the disclosed device uses no recesses below the spacer voids 232 and 234. There are simply no voids underneath spacers 224 and 226. Accordingly, as the Examiner correctly acknowledged, YU cannot be read to disclose or suggest filling a first portion of the recesses with a stress imposing material and filling a second portion of the recesses with a semiconductor material (claim 1).

Furthermore, as explained above, while Applicants acknowledge that GARDNER discloses a device which forms LDD areas 48 within spacer openings 46 and in the substrate 30 (see col. 7, lines 41-56 and Figs. 7-17), GARDNER does not disclose recesses arranged below spacer voids 46. Again, reference numbers 48 in Fig. 9 of GARDNER are disclosed as being formed LDD areas (see col. 7, lines 41-56) and not recesses. Moreover, as correctly acknowledged by the Examiner, GARDNER fails to

disclose or suggest filling a first portion of the recesses with a stress imposing material and filling a second portion of the recesses with a semiconductor material (claim 1).

However, as noted above, MURTHY does not cure the deficiencies of YU and GARDNER. While it is apparent that MURTHY discloses a device having recesses 36A and 36B with surfaces 38 and that are filled with materials 40A and 40B (see Figs. 5-6 and col. 3, lines 27-59), it is clear that the recesses 36A and 36B are not arranged below spacer voids. To the contrary, MURTHY discloses spacers 26A and 26B which have regions 22A and 22B underneath. There are no voids underneath spacers 26A and 26B. Accordingly, the Examiner simply cannot properly argue that MUTHRY discloses or suggests filling a first portion of the recesses with a stress imposing material and filling a second portion of the recesses with a semiconductor material (claim 1).

Accordingly, Applicants submit that no proper combination of YU, GARDNER and MURTHY discloses or suggests the combination of features recited in at least claim 1.

Moreover, in addition to failing to disclose the combination of features recited in the above-noted claim 1, Applicants submit no proper combination of these documents discloses or suggests the combination of features recited in dependent claims 19-22, which also respectfully contain all of the features of claim 1.

Accordingly, Applicants respectfully submit that the above-noted rejection under 35 U.S.C. § 103(a) should be withdrawn.

Over Yu with Murthy

Claims 38-47 were rejected under 35 U.S.C. § 103(a) for being allegedly unpatentable over YU in view of GARDNER. This rejection is respectfully traversed.

The Examiner acknowledges that YU fails to disclose, among other things, etching recesses into the semiconductor substrate at a bottom of the spacer voids, introducing a compressive or tensile imposing material into a portion of the recesses, and filling a remainder of the recesses with material. However, the Examiner explains that these features are taught by MURTHY and that it would have been obvious to combine the teachings of these documents.

Applicants respectfully submit that a *prima facie* case of obviousness has not been established as the applied references fail to teach each and every element of the claims.

As explained above, while it is apparent that YU discloses a device having regions 210/214 and 242/244 below spacer voids 232 and 234 (see Figs. 6-8), it is clear from Figs. 6-11 that the layers 228 prevent the spacers from penetrating into the substrate and that the disclosed device uses no recesses below the spacer voids 232 and 234. There are simply no voids underneath spacers 224 and 226. Accordingly, as the Examiner correctly acknowledged, YU cannot be read to disclose or suggest etching recesses into the semiconductor substrate at a bottom of the spacer voids, introducing a compressive or tensile imposing material into a portion of the recesses, and filling a remainder of the recesses with material (claim 38).

However, as noted above, MURTHY does not cure the deficiencies of YU. While it is apparent that MURTHY discloses a device having recesses 36A and 36B with

surfaces 38 and that are filled with materials 40A and 40B (see Figs. 5-6 and col. 3, lines 27-59), it is clear that the recesses 36A and 36B are not arranged below spacer voids. To the contrary, MURTHY discloses spacers 26A and 26B which have regions 22A and 22B underneath. There are no voids underneath spacers 26A and 26B. Accordingly, the Examiner simply cannot properly argue that MUTHRY discloses or suggests etching recesses into the semiconductor substrate at a bottom of the spacer voids, introducing a compressive or tensile imposing material into a portion of the recesses, and filling a remainder of the recesses with material (claim 38).

Accordingly, Applicants submit that no proper combination of YU and MURTHY discloses or suggests the combination of features recited in at least claim 38.

Moreover, in addition to failing to disclose the combination of features recited in the above-noted claim 38, Applicants submit no proper combination of these documents discloses or suggests the combination of features recited in dependent claims 39-47, which also respectfully contain all of the features of claim 38.

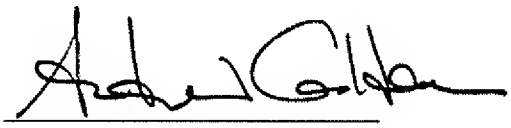
Accordingly, Applicants respectfully submit that the above-noted rejection under 35 U.S.C. § 103(a) should be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submit that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number

listed below, if needed. Any fees required for consideration of the instant response are hereby authorized to be charged to our Deposit Account No. 09-0458.

Respectfully submitted,
Michael P. Belyansky, *et al.*



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